The AMD Athlon™ Processor: Architectural Enhancements for Advanced Multiprocessor Systems

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Agenda

- **Symmetric Multiprocessor (SMP) System Requirements**
- **The AMD SMP Solution:**
  - AMD Athlon™ Processor
    - Advanced Cache Architecture
    - System Bus Architecture
  - AMD-760™MP Chipset
    - Advanced System Features
    - DDR Memory Technology

SMP System Requirements

- **Microprocessor Core**
  - Advanced Microarchitecture for MP operating systems and multi-threaded applications
  - Superscalar Floating-point Engine for computational intensive applications
  - On-die, full speed Advanced Cache Subsystem
- **Processor Front-Side Bus (FSB)**
  - Bus protocol provides the highest level of sustained bandwidth
  - Reliable, large burst transfers
  - Snoop traffic does not impact performance
- **Memory Subsystem**
  - Memory interface provides the highest level of sustained bus bandwidth
  - Cost-effective
  - Availability
- **Chipset**
  - Maximum memory bandwidth for processors and graphics to system memory
  - Maximum system transaction concurrency
  - More efficient memory coherency protocol

AMD Athlon™ Platform: *Bandwidth Realization*

AMD Athlon™ Processor

- 7th generation, high speed processor core
- Superscalar Floating Point Engine
- On-die, full speed advanced cache subsystem with:
  - Multi-level TLB's
  - Largest L1 cache (128kB)
  - Large L2 caches (256kB+)
  - First x86 MOESI cache coherency protocol

Processor Front-Side Bus

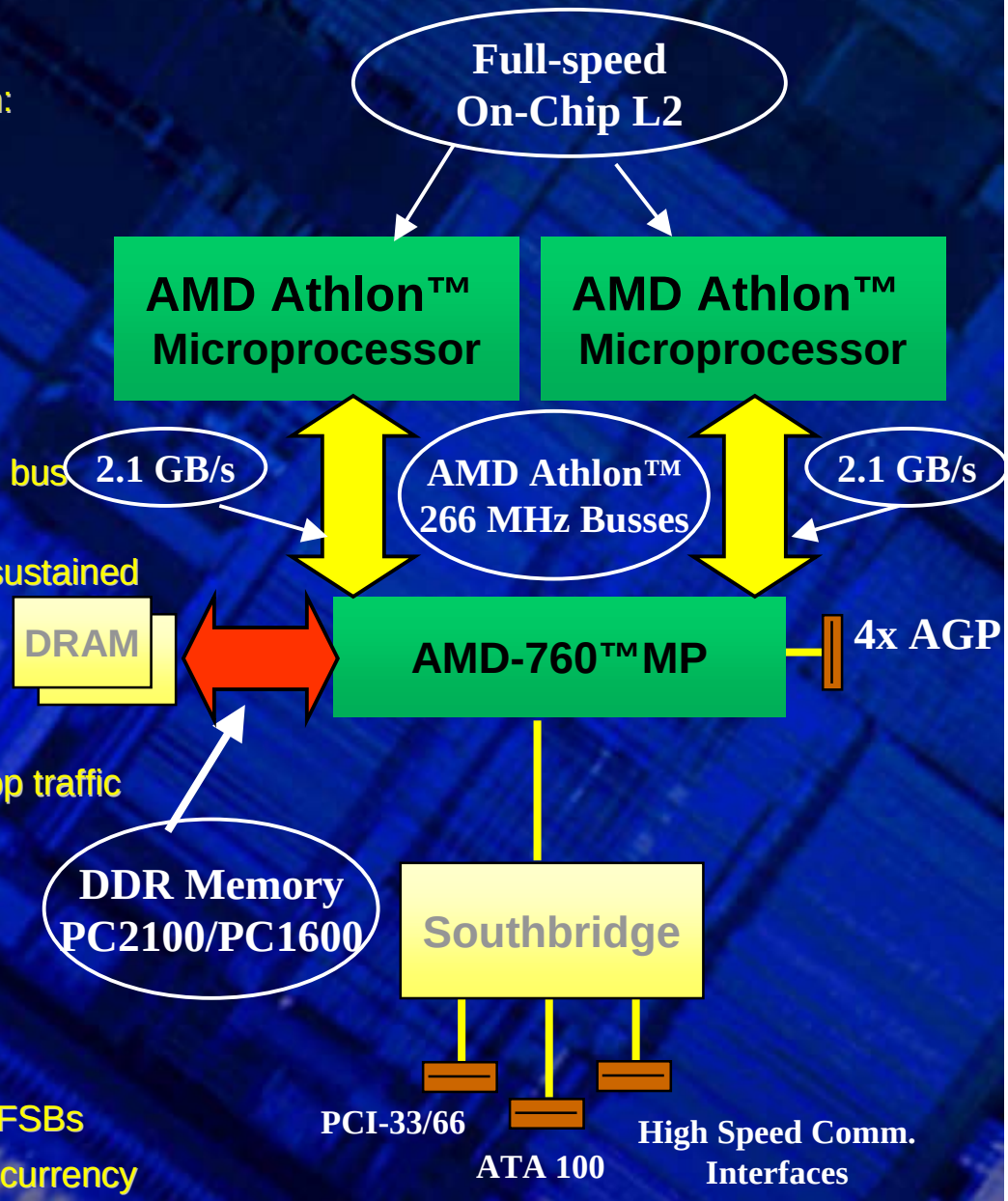
- Point-to-Point (non-sharing) topology
- Provides over 4.2 GB/s (@266MHz) of sustainable bus bandwidth for a 2P system
- Bus protocol optimized to provide highest level of sustained bus bandwidth
- Source synchronous clocking for high frequencies
- Large 64 byte burst transfers
- Dedicated Snoop bus eliminates address bus snoop traffic

PC2100 & PC1600 DDR SDRAM Memory

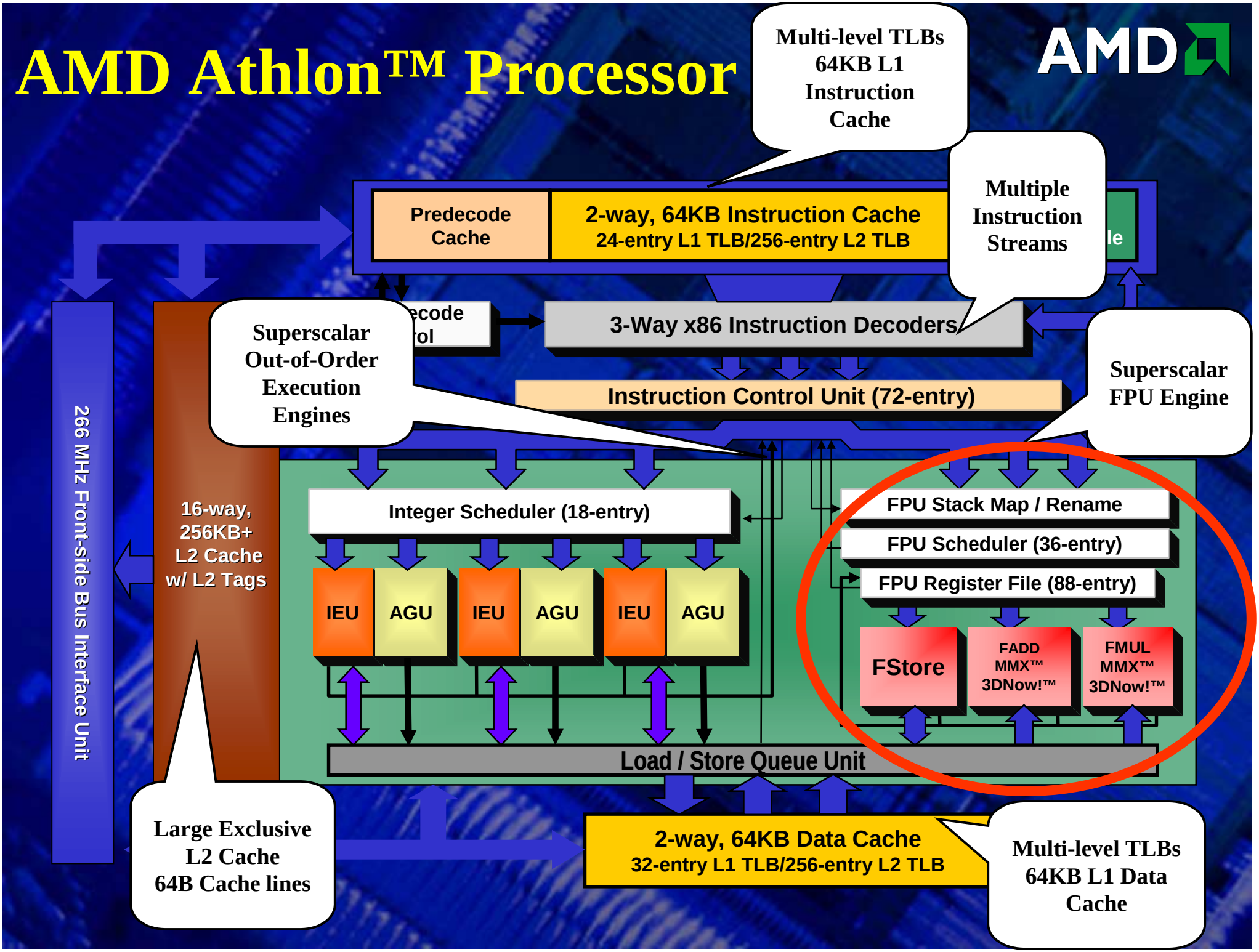
- High Bandwidth (2.1 GB/s) and low latency
- Available and cost-effective for most solutions

AMD-760™ MP Chipset

- Two 266MHz (2.1 GB/s) AMD Athlon™ processor FSBs
- Advanced buffering for maximizing transaction concurrency
- MOESI cache coherency protocol increases memory bandwidth utilization



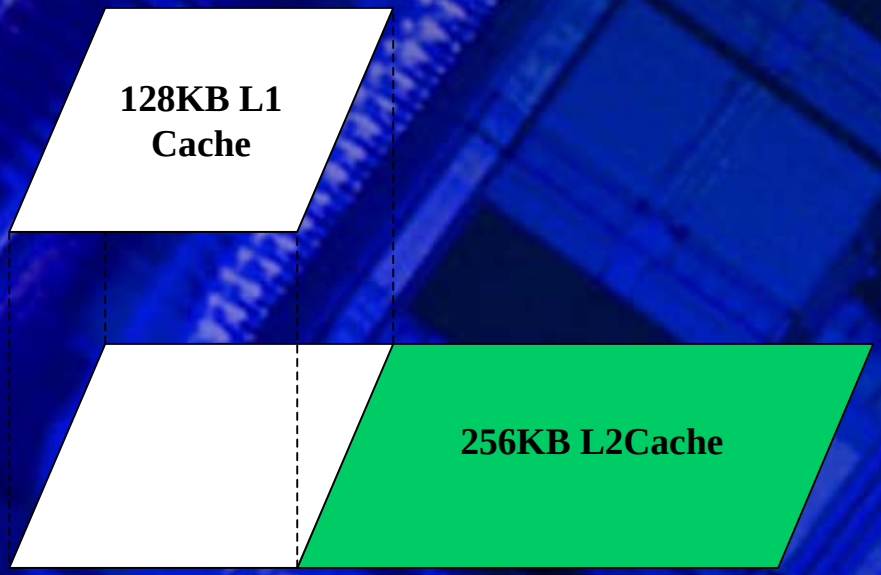
AMD Athlon™ Processor



L2 Cache: Exclusive vs. Inclusive

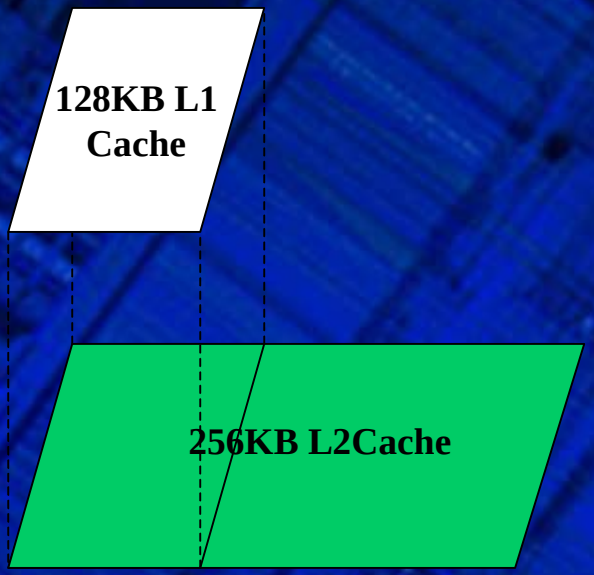
AMD Athlon™ Processor

Exclusive



Total Size = 256KB L2 + 128KB L1 = 384KB

Inclusive

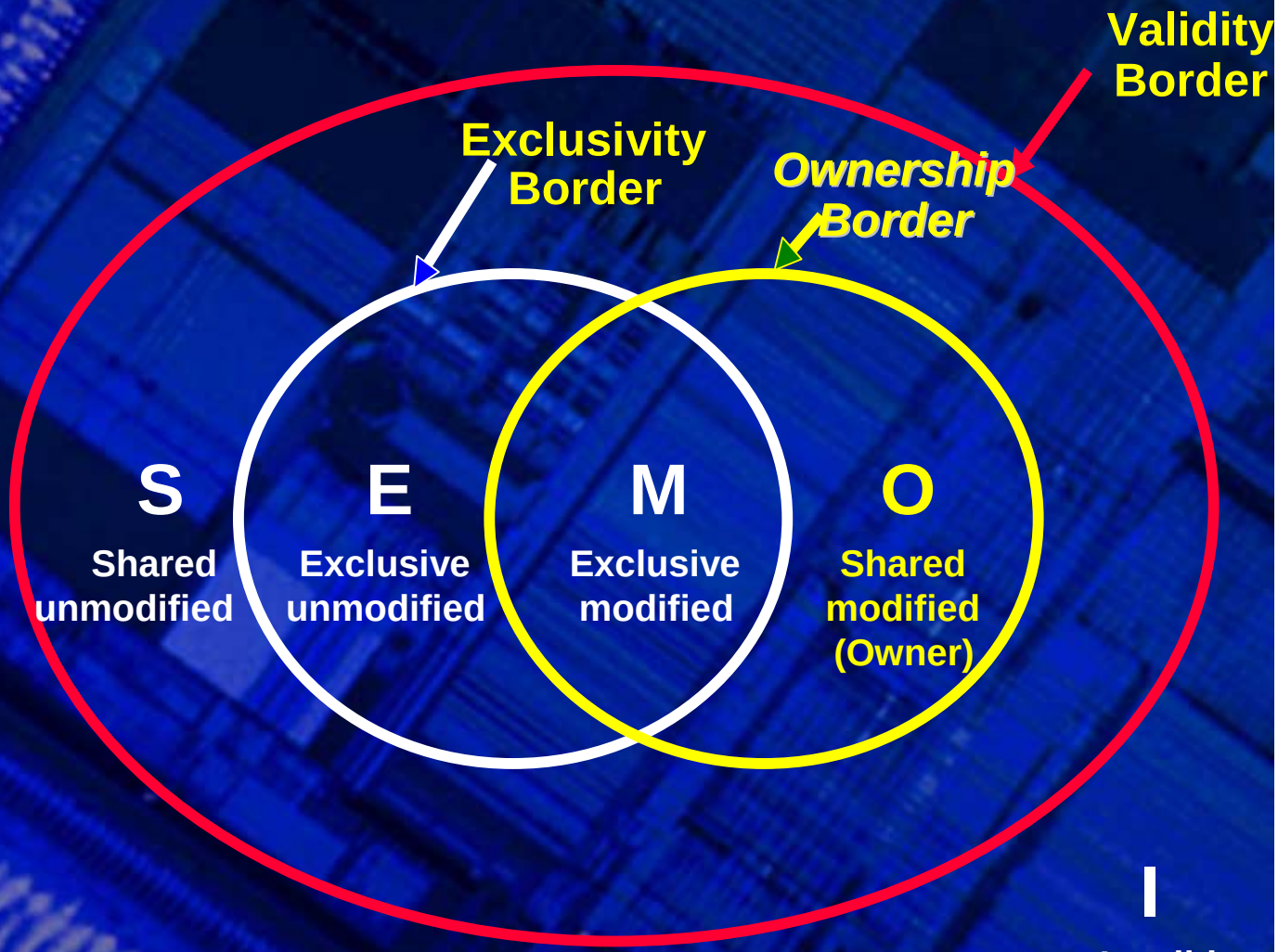


Total Size = 256KB L2 +/- 128KB L1 = 256KB

- Greater effective cache size from exclusive architecture with the AMD Athlon™ processor.
- Dedicated L1 snoop port to service probe requests without interfering with L1 loads and stores.

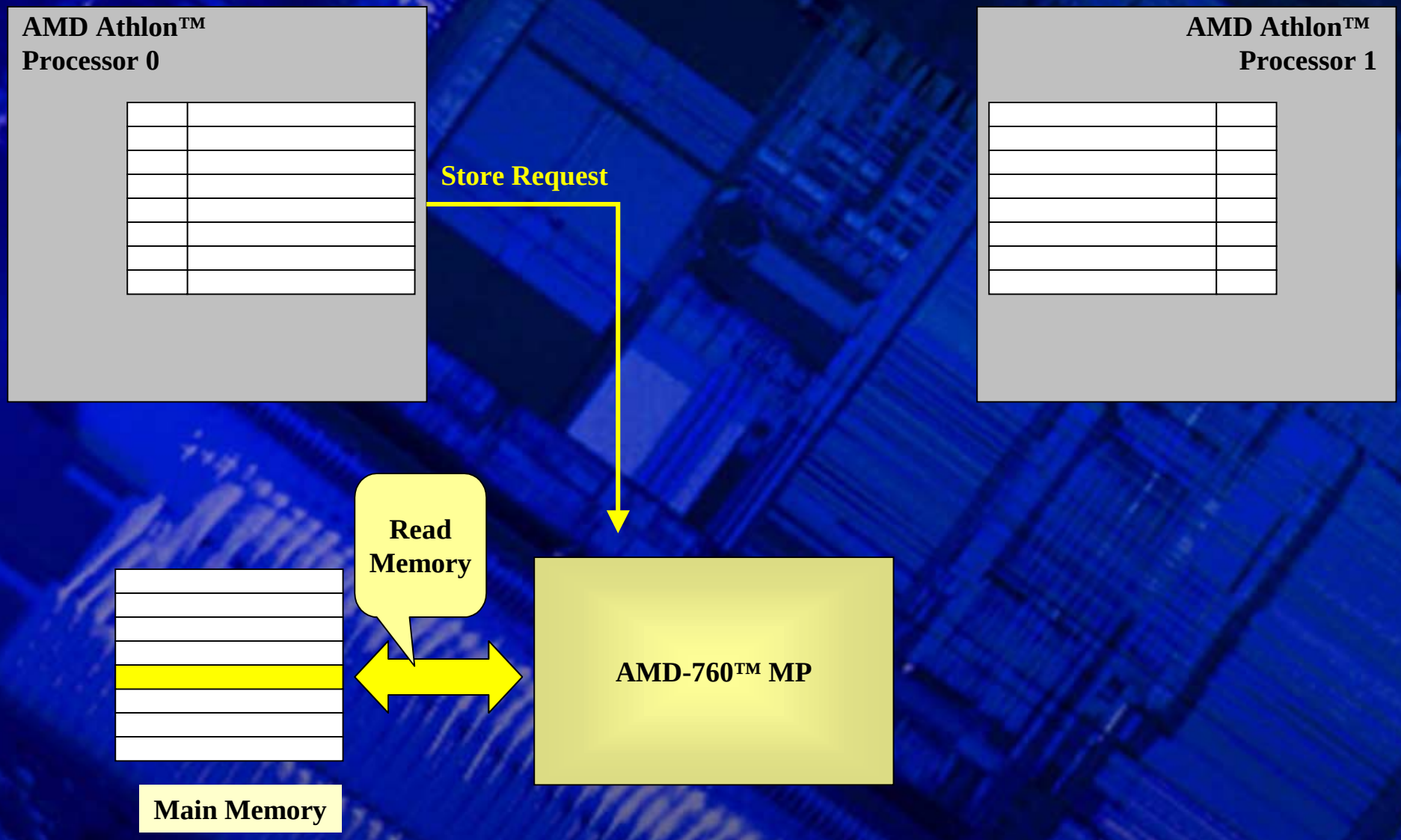
MOESI Cache Coherency

- **E - Exclusive**
  - cache line same as memory
  - no other CPU has this cache line
- **M - Modified**
  - modified cache line
  - no other CPU has this cache line
- **S - Shared**
  - cache line same as memory and other CPUs
- ***O - Owner***
  - ***cache-to-cache transfer eliminates cache line thrashing***
  - ***significantly saves memory bandwidth***
  - ***modified cache line shared with other CPUs***
  - ***owner must update memory***



MOESI and P2P-bus Topology

Example: Two Processors sharing modified data



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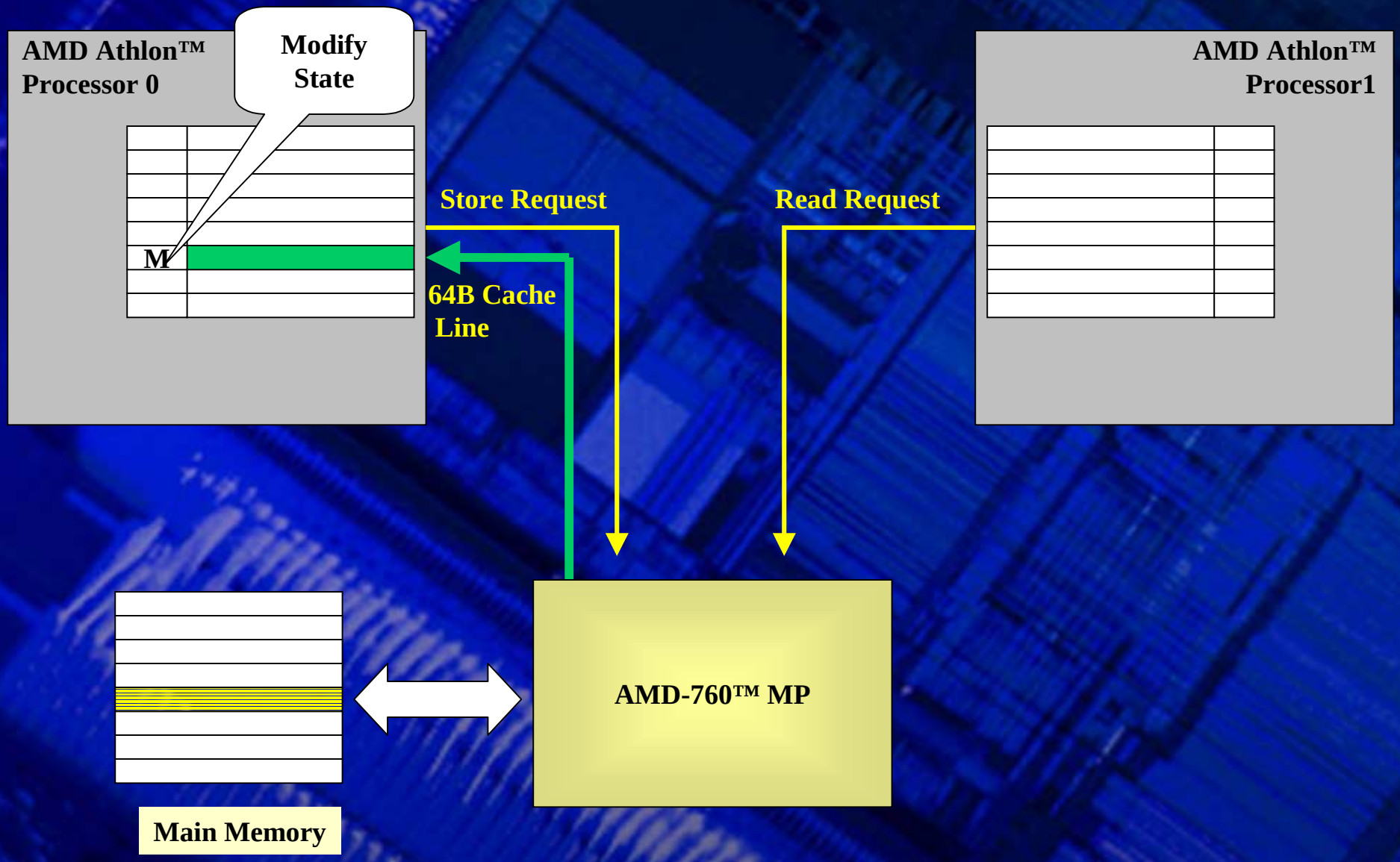

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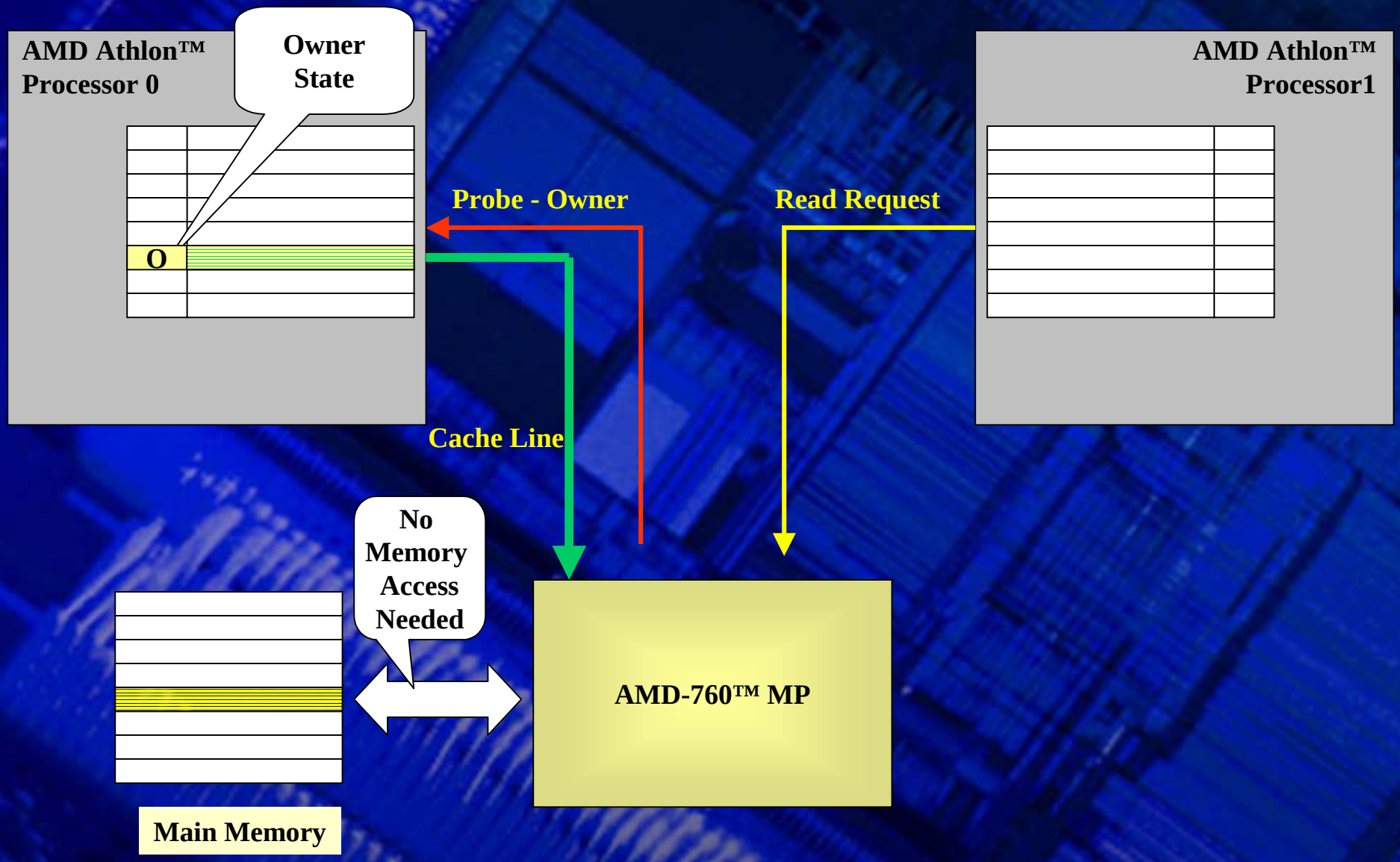

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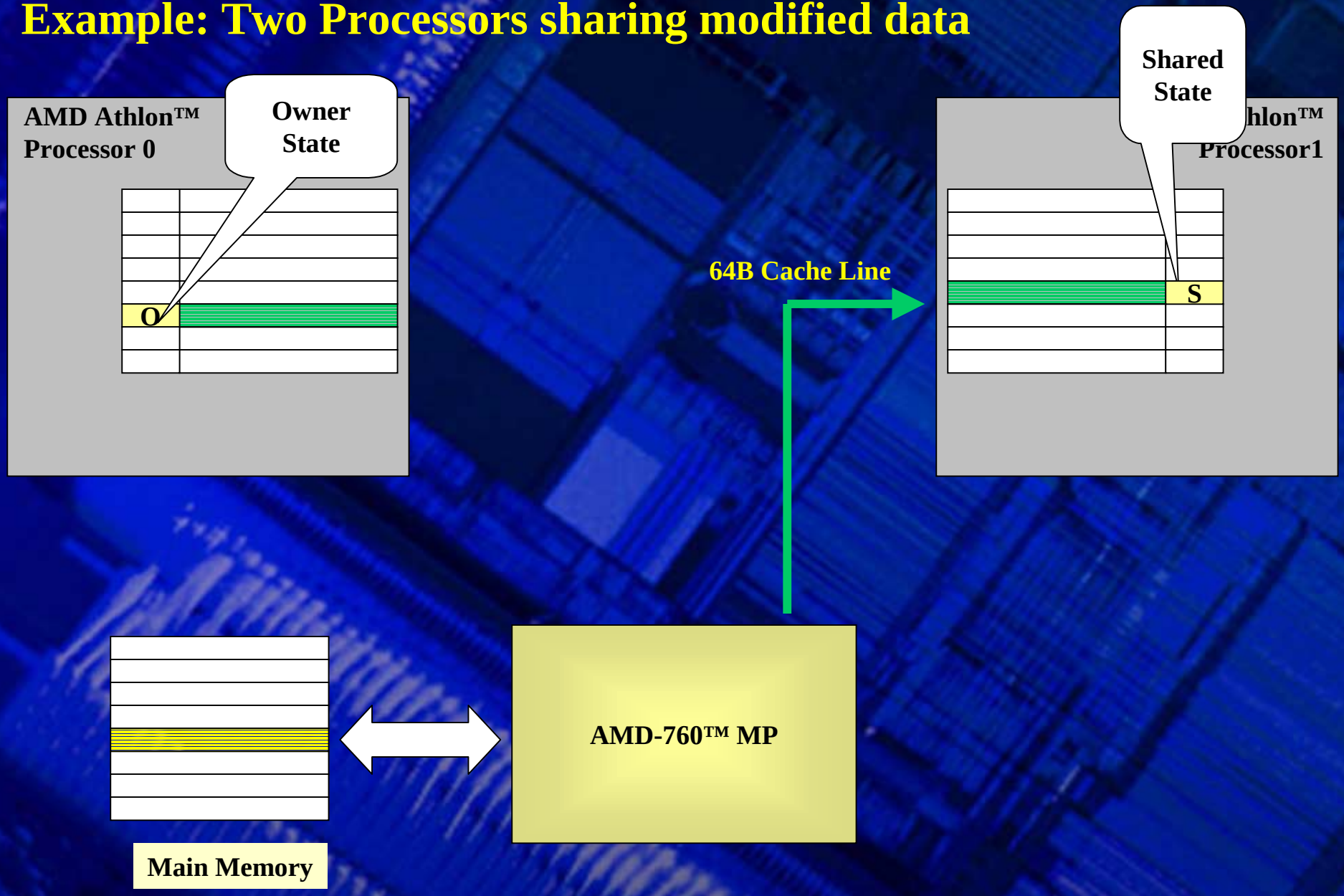

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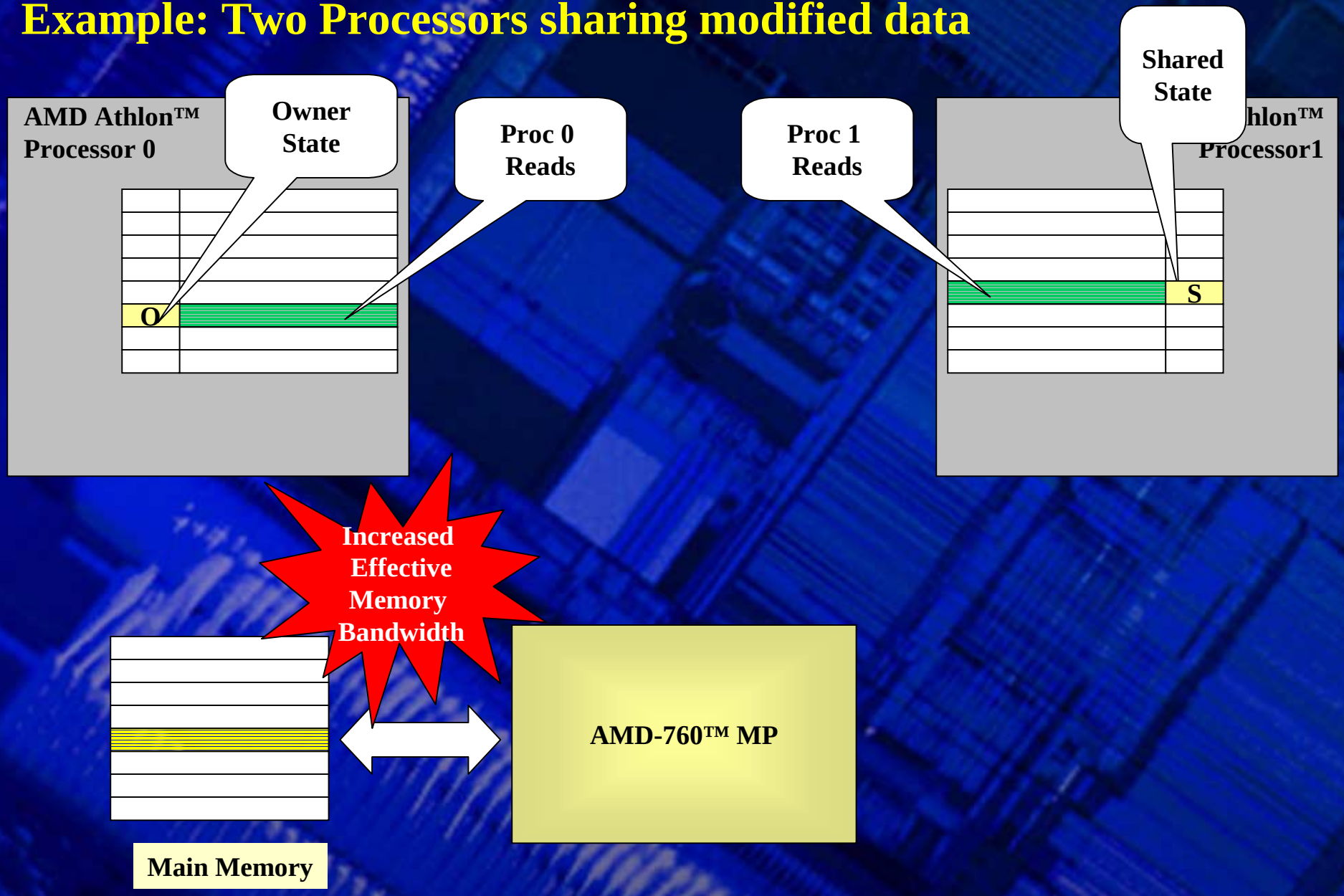
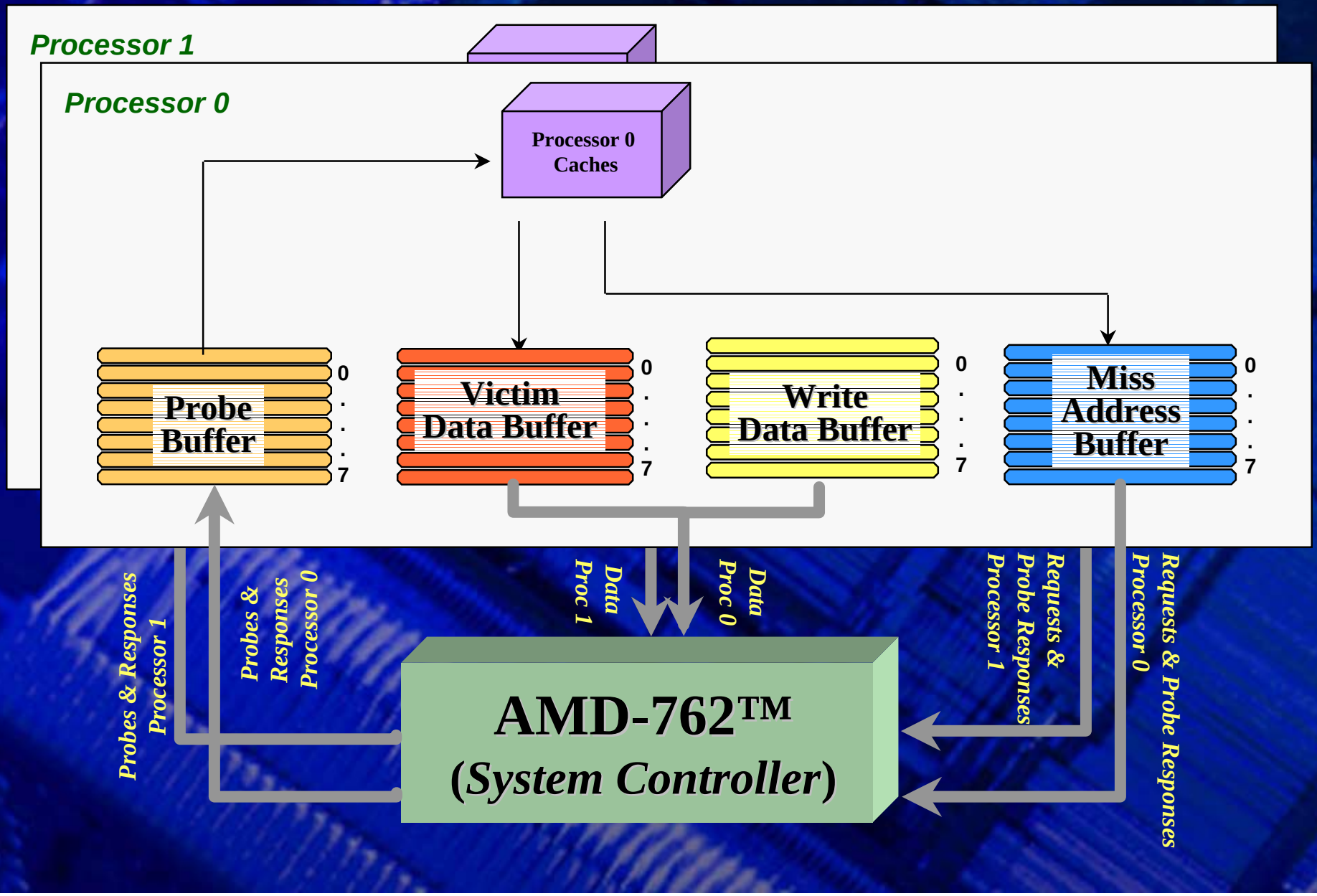


AMD Athlon™ System FSB Architecture

- **AMD Athlon™ System Bus Architecture - *Scalable and Flexible***
  - Defined for 6.4GB/s (@400MHz) sustainable data transfer rate in a 2P system
  - Split-transaction, packet-based MP bus protocol for high efficiency and low pin counts
  - Defined for 43 physical address bits for up to 8 terabytes of physically addressed memory
  - Point-to-Point connections that reduce typical bus loading and topology limits
  - Clock Forwarding reduces insidious clock skews and delay (physics) limits
  - Simultaneous, independent (*non-intrusive*) busses for commands, snoops and data
  - ECC Multi-bit detection and single-bit correction
  - Low voltage, push-pull signaling technology
- **AMD Athlon™ Processor Today**
  - 2.1GB/s today with 266MHz FSB
  - 35-bit physical addressable memory
  - 72-Bit Bi-directional Data Bus (64bit data+ 8bits ECC)
  - 24 outstanding data transactions plus up to 8 outstanding probes
  - AMD Socket-A Infrastructure

Transaction Concurrency



AMD-762™ System Controller

Designed for:

- **Support of two AMD Athlon™ processors on 266MHz FSB**
  - Over 2.1 GB/sec transfer rates at 266MHz per processor
  - Large 64-byte burst transfers
  - MP bus protocol
  - Point-to-Point FSB Topology
- **Optimized MOESI Cache Coherency Protocol**
  - Chipset controls all system memory coherency states
  - MOESI reduces memory bandwidth requirements for Shared-Modified data
- **PC-2100 DDR DRAM Interface**
  - Customer requested
  - Cost-effective
  - Widely available
  - Over 2.1 GB/sec transfer rates
  - Supports up to 4GB of memory
- **4X-AGP Interface (Supports 1X, 2X, 4X modes).**
- **Host/PCI Bus Bridge (Supports 33MHz/66MHz and 32/64-bit modes independently).**

AMD-762™ System Controller

DDR Memory Controller Features

Designed to:

- **Support the following concurrencies.**
  - Processor-to-main-memory with PCI-to-main-memory.
  - Processor-to-main-memory with AGP-to-main-memory.
  - Processor-to-PCI with PCI-to-main-memory or AGP-to-main-memory.
- **Support ECC (Error Correcting Code) and scrubbing.**
- **Support 2, 2.5, and 3 CAS Latencies.**
- **Support the following DRAM.**
  - Support 4 Registered DIMMs.
  - Supports 64Mb, 128Mb, 256Mb, and 512Mb Technology.
  - 64-bit data width, plus 8-bit ECC paths.
  - Flexible row and column addressing.
- **Support up to 4 GB of memory.**

DDR is an Evolutionary Upgrade

- **Responding to AMD Customers**
  - Leading PC OEMs requesting most favorable cost model for expanded memory bandwidth
  - AMD-760™ DDR chipsets set for 2H'00 intro with AMD-760™MP to follow
- **DDR offers Market Leading Performance**
  - Low latency and high bandwidth (*up to 2.1 GB/sec*) = Strong performance
  - Natural migration from PC133 SDRAM - Similar manufacturing and test infrastructure
- **DDR Gains Broad Industry Support**
  - DDR is available from every major DRAM supplier in the world:
    Micron, Hitachi, Hyundai, IBM, Infineon, Mitsubishi Electric, NEC, Samsung, Toshiba
  - TeamDDR Marketing Initiative launched: www.teamddr.com
  - AMD supports DDR initiative: www.amd.com/devconn/teamddr.html
  - DDR has broad support from both motherboard and chipset vendors
- **Cost-effective**
  - Similar protocols and design methodologies to SDRAM
  - JEDEC Standard I/O drivers
  - Same manufacturing infrastructure
  - Standard TSOP Packaging
- **Serves all markets**

Summary

- **Together, the AMD Athlon™ processor, AMD-760™MP chipset, and DDR memory technology remedy bottlenecks associated with existing x86 MP solutions. Revealing a new platform that more closely models that of the ideal x86 MP solution.**
  - Superscalar, fully pipelined Floating Point Unit
  - Largest, most advanced L1 cache memory
  - Large, exclusive L2 cache memory
  - MOESI cache coherency
  - Point-to-Point bus transfers to maintain bus bandwidth when scaling
  - 266 MHz FSB
    - high bandwidth @ 2.128 GB/s
    - high transaction concurrency
  - 266 MHz DDR memory technology
    - high bandwidth @ 2.128 GB/s
    - low latency
    - Cost-effective & available
- **The AMD Athlon™ processor and the AMD-760™MP chipset enable the next generation of high performance x86 multiprocessing systems.**

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